A New Topology of Single Phase Inventive Multilevel Inverter Analysis of Matlab Simulation

N. Sundaramurthy[1*] and S.Rajalakshmi[2]

[1*]Department of Physics,Annamalai University,Annamalai Nagar. Post Graduate and Research Department of Physics, Thiru Kolanjiappar Government Arts College, Vriddhachalam, 606001. [2]Department of Physics, University College of Engineering Panruti, Anna University.

ABSTRACT

Multilevel inverters have been developed to handle high power and high voltage in the flexible power systems. These inverters offer some inherent advantages over conventional 2-level inverters. High quality of the output voltage of the multilevel inverters is one of the most important advantages. Though the multilevel inverters hold attractive features, usage of more switches in the conventional configuration poses a limitation to its wide range application. The emphasis is on reducing the number of switches, which inturn reduces switching losses, and avoiding the capacitors, which may likely to cause voltage imbalance, and using less number of DC sources, which may increase additional isolation Transformer requirements, while designing a new prototype. A review has been done on the recently proposed topologies. A control strategy is proposed in this paper to minimize total harmonic distortion (THD). In this paper, a new topology of cascaded multilevel inverter using a least number of switches is designed with R&RL load for high voltage applications. The objective is to reduce the number of switches with minimum harmonic distortion to attain high voltage capability, harmonic filtering in power systems, etc. In short, the cascade inverter is much more efficient and suitable for utility applications than traditional multi-pulse and pulse width modulation (PWM) inverters. Two determinations have been presented here to show the comparison in THD values. The Validity of the analysis has been proved by simulation using MATLAB.

KEYWORDS: Multilevel inverter, Cascaded multilevel inverter, Full-bridge, H-bridge.

*Corresponding author:

Dr. N. Sundaramurthy

Post Graduate and Research Department of Physics,

Thiru Kolanjiappar Government Arts College,

Vriddhachalam, 606001.Tamil nadu-India.

Email:nagasundaramphysics@gmail.com. Mobile:+91-9976994921.

INTRODUCTION:

Multilevel inverter technology is a very efficient alternative for medium-voltage and high-power applications because of its fruitful advantages. It can realize high voltage and high power output by using semiconductor switches without the use of transformer and dynamic voltage balance circuits. When the number of output levels increases, the harmonic content in the output voltage and current decreases. The basic concept of a multilevel inverter is to achieve high power by using a series of power semiconductor switches with several lower DC voltage sources to perform the power conversion by synthesizing a staircase voltage waveform. To obtain a low distortion output voltage nearly sinusoidal, a triggering signal should be generated to control the switching frequency of each power semiconductor switch. In the proposed study the triggering signals to multilevel inverter (MLI) are designed by using the Hysteresis current control technique. The well-established topologies of multilevel inverters include neutral point clamped (NPC), flying capacitor and Cascaded Multilevel Inverter (CMLI). These inverters have several advantages over the traditional inverters. The CMLI configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications. The CMLI is designed with a series of H-bridge (single-phase full bridge) inverter units.

This paper suggests a new topology for cascaded multilevel inverters with a high number of steps associated with a low number of switches switches. In addition, for producing all levels (odd and even) at the output voltage, three procedures for calculating the required dc voltage sources are proposed. Finally, the paper includes simulation results to prove the feasibility of the proposed multilevel inverter.

Cascaded multilevel inverter:

These are of full-bridge configuration with SDCS, which may be batteries, fuel cells or solar cells and are connected in series .Each FBI unit can generate a three level output: $+V_{dc}$, 0 or $-V_{dc}$ by connecting the DC source to the AC load by different combinations of the four switches of each FBI. Using the FBI as the example, turning on S_{11} and S_{41} yields $+V_{dc}$ output. Turning on S_{21} and S_{31} yields $-V_{dc}$ output.

Turning off all switches yields '0' volts output. The AC output voltage at other FBIs can be obtained in the same manner. The number of voltage levels at the load generally defines the number of FBIs in cascade. The number of FBI units or DC sources N is (m-1)/2 where m is the sum of zero level and the number of positive and negative levels in MLI output. Each switching component turns on and off only once per cycle i.e. at the line frequency.The cascaded multilevel inverter consists of series connections of n full bridge topology. Fig.1 shows the configuration of cascaded multilevel inverter.
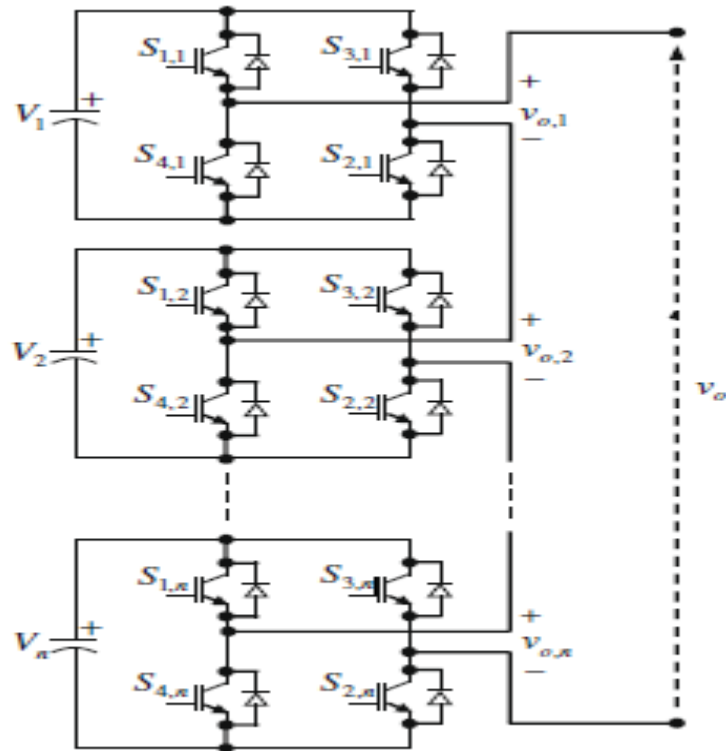
Fig. 1. Configuration of cascaded multilevel inverter.

The ouput voltage of mulitilevel inverter is given by

$V_0 = V_{0,1} + V_{0,2} + \ldots + V_{0,n}$

In symmetric MLI the number of full bridges(n) is given by

$N_{step} = 2N + 1$

SUGGESTED TOPOLOGY:

Single Phase Full Bridge Inverter:

From the fig.2. Shows the single phase full bridge inverter with R load.In that fig.2. there are four switches(SA,SB,SC,SD) connected across load with dc supply.during positive half cycle,SA and SB will turn on and other turn off.then the load flows through it and produce $+V_{dc}$ .During negative half cycle,SC and SD will turn on and two turnoff.and it produce $-V_{dc}$ .then if all switches are on,there will be 0V produced.
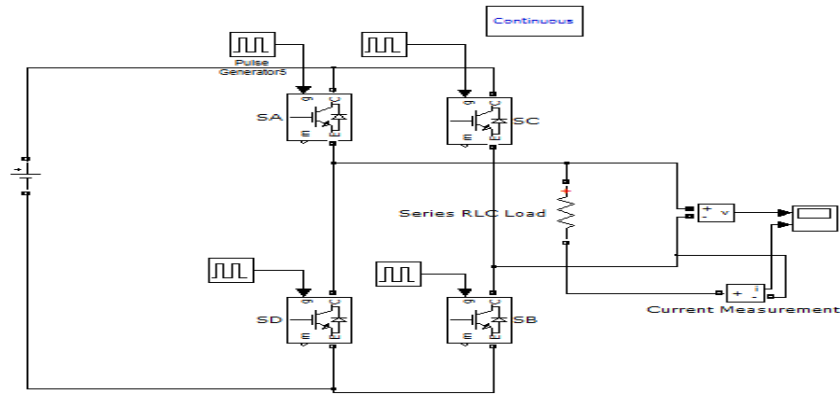
Fig.2:Single Phase Full Bridge Inverter With R Load

Now the same full bridge inverter is connected with RL load with a power factor of 0.8(lag).the fig.3.shows the single phase full bridge inverter with RL load.
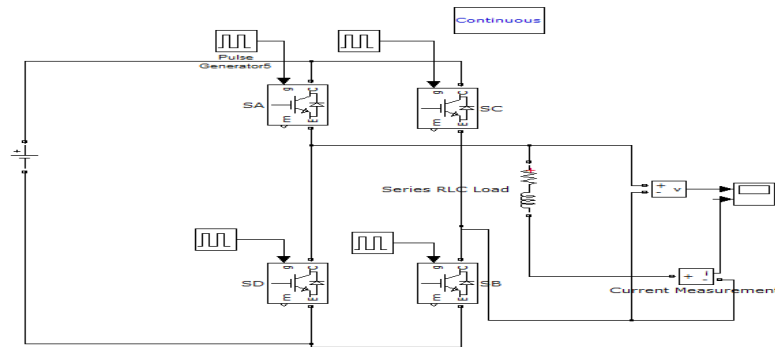

Fig.3:.Single Phase Full Bridge Inverter With RL Load.

Table.1.Specification Of Five Level Multilevel Inverter.

PARAMETERS NAME	VALUE
INPUT VOLTAGE	12V
OUTPUT VOLTAGE	24V
OUTPUT POWER	200W
POWER FACTOR	0.8 &0.6(lag)

From the tabulation, the values are implemented in five level mulitilevel inverter,by using the below fig.4. Shows the five level multi level inverter with R load.
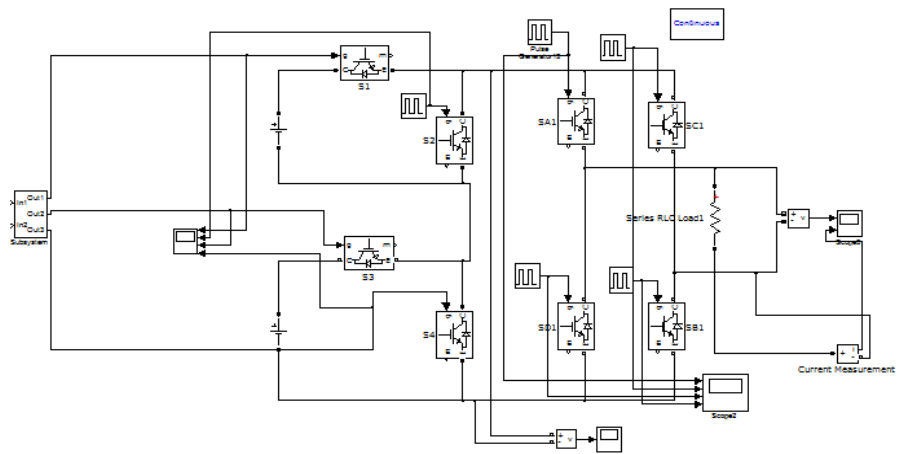
Five Level Multi Level Inverter:

Fig.4. Five Level Multi-Level Inverter With R Load

From the fig.4. it contains (S1,S2,S3,S4 and SA,SB,SC,SD) has eight switches, connected with dc supply and load connected across in it. the operations are during +vdc S1 &S4 and SA1 &SB1 turns on, others in turns off. During +2vdc S1 &S3 and SA1& SB1 turns on while others in turns off. Similarly the negative cycle to be repeated vice versa respectively.Similar to resistive load, the inductive load is added with a power factor of 0.8(lag),the fig.5.shows the five level MLI with RL load respectively.
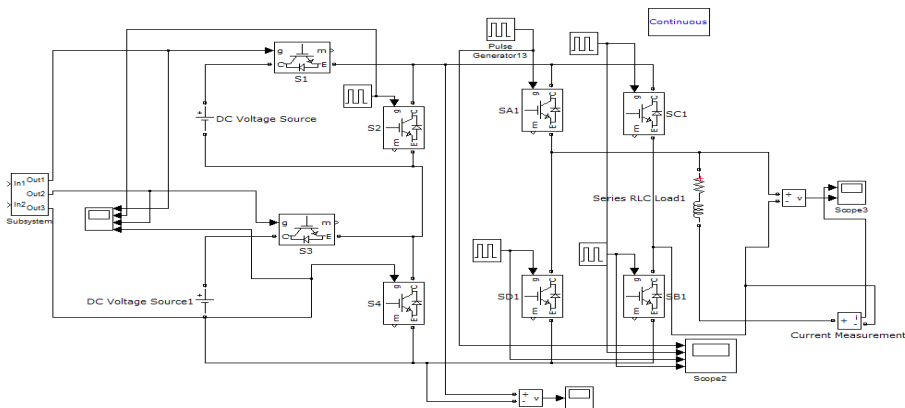

Fig.5. Five Level Multi Level Inverter With RL Load

Design: From the given parameter value, find the current value, from the below given equation,

P = VI cos ϕ

From the power triangle calculations,

cos ϕ = R/Z

Then calculate the inductance value by using the formula

X_L = 2ΠFL

Then to find the real &reactive power,

P = VI cos ϕ and Q=VI sin ϕ.
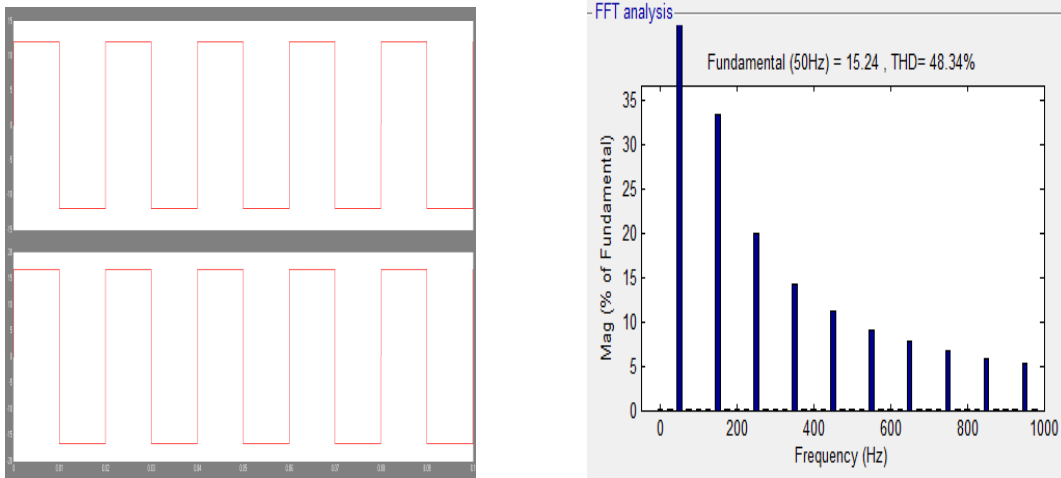
MATLAB Simulation Results:

Fig. 6. Typical Output Voltage And Current Wave Forms Of Single Phase Full Bridge Inverter With R Load And Their FFT Spectrum.

From the fig.6.it shows the output voltage and current waveforms and their total harmonic distortion as 44.15%.now compare with RL load.
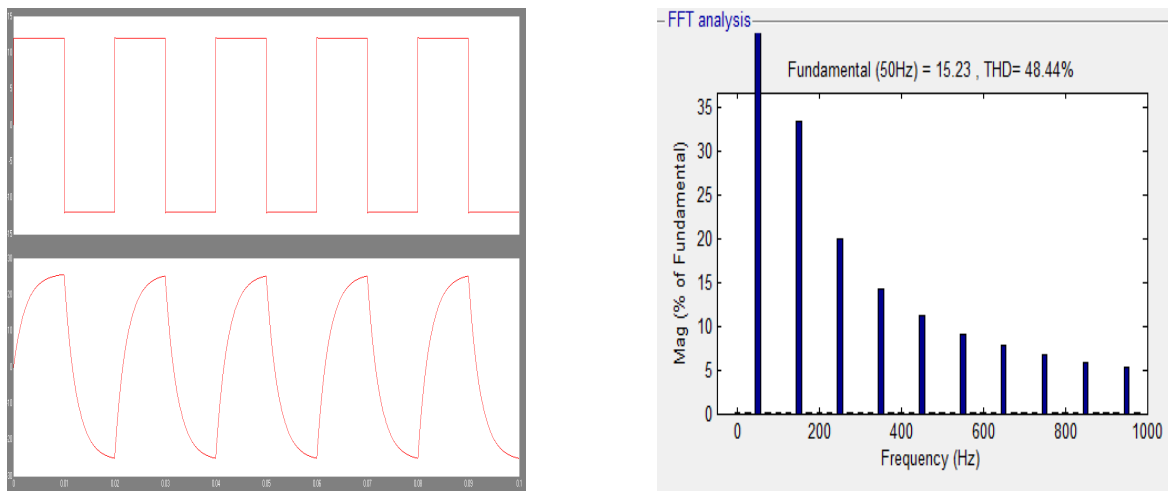

Fig. 7. Typical Output Voltage And Current Wave Forms Of Single Phase Full Bridge Inverter With RL Load And Their FFT Spectrum.

From the fig.7 shows the full bridge inverter with RL load has been showed respectively. Now compare with five level multilevel inverters with R load. Fig.8.shows the output waveforms for R load.
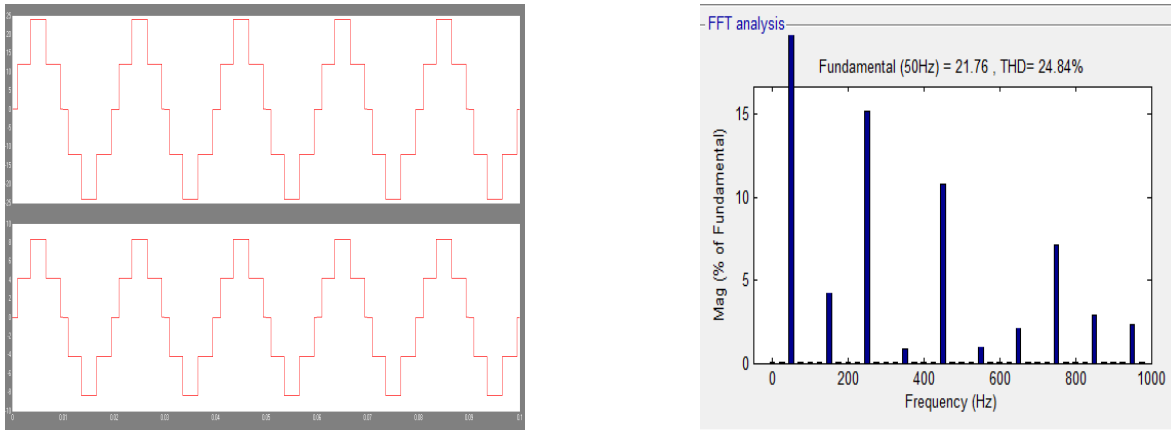
Fig. 8. Typical Output Voltage And Current Wave Forms Of Five Level With R Load And Their FFT Spectrum.

Now compare with five level MLI with RL load with 0.8 pf ,the ouput current waveforms will be like charging & discharging respectively from the fig.9
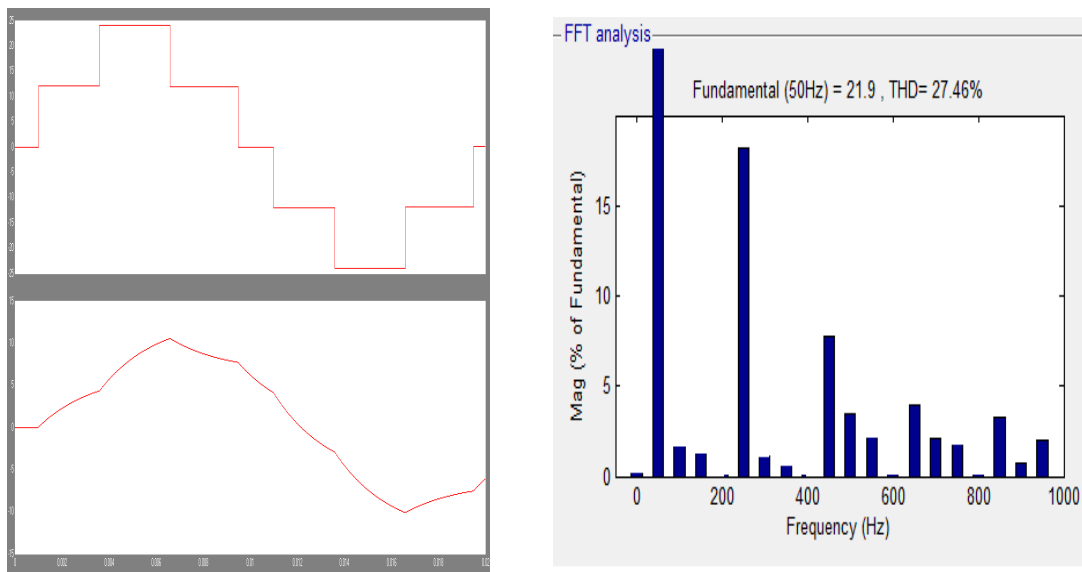

Fig. 9: Typical output voltage and current wave forms of five level with RL load and their FFT spectrum.

Now there is a comparison between single phase and five level multilevel inverter, when compared to five level inverter the THD value is less than that of single phase full bridge inverter.so when the number of level increases, the output voltage waveforms becomes a staircase, which approaches minimum harmonic distortion accordingly.

From the fig .6 and fig.8. can see the differences with the values get decreased when compared to 8 and 4 switches. The THD values also calculated theoretically, that also presented here to scope the variations in values.

PRACTICAL THD VALUE (%) R LOAD	THEORETICAL THD VALUE (%) R LOAD
[Single Phase Full Bridge Inverter] **44.15**	**44.33**
[Five Level MLI] **26.33**	**26.76**

Table.2.Comparison of THD values in single phase and five level multi level inverter.

CONCLUSION:

A new configuration of cascaded multilevel inverter has been proposed. From the above simulation result, we can get an clear idea that, As the number of levels increases, the output voltage that can be spanned by summing multiple voltage levels also increases. MLIs have many attractive features like high voltage capability, reduced common mode voltages, near sinusoidal outputs, making the inverters suitable for high power applications. As the number of voltage levels increases, the harmonic content of the output voltage decreases significantly.

REFERENCES

1. Babaei E.A, "Cascade multilevel converter topology with reduced number of switches", IEEE Trans Power Electron, 2008;23(6): 6.
2. Baker RH."Electric power converter".US Patent 03-867-643;1975.
3. Rodriguez J,Lai JS, Peng FZ," Multilevel inverters: survey of topologies controls, and applications". IEEE Trans Ind Appl 2002;49(4):724-38.
4. Du Z, Tolbert Lm,Chiasson JN." Active Harmonic elimination for multilevel converters". IEEE Trans Power Electron 2006;21(2):459-69.